REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1-5 and 16-18 under 35 USC § 103 (a) as being unpatentable over Weber (U.S. Patent No. 6,504,433) in view of Yamaguchi (U.S. Patent No. 6,804,500) and further in view of Vathulya (U.S. Patent No. 6,636,119); and claims 6-15 under 35 USC § 103 (a) as being unpatentable over Weber (U.S. Patent No. 6,504,433) in view of Yamaguchi (U.S. Patent No. 6,804,500) and Vathulya (U.S. Patent No. 6,636,119) and further in view of Hans (U.S. Patent No. 5,923,215).

Claims 1-18 are currently pending in this application. Claims 1, 8, 12 and 16 have been amended to more distinctly claim and to more particularly point out Applicant's invention. The rejections and objections above have been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1-18.

2. Claim 1 was rejected under 35 USC § 103 (a) as being unpatentable over the combination of Weber, Yamaguchi and Vathulya. In setting forth the rejection, the Examiner cited Weber as disclosing the first transistor pair of claim 1 based on transistors (12) and (14) of Weber's Fig. 1. Claim 1, as amended now recites:

> first transistor pair coupled in series with the component, wherein a first transistor of the first transistor pair is coupled to receive an input signal and wherein a second transistor of the first transistor pair is coupled to receive a first enable signal and is configured to enable the first transistor of the first transistor pair when the first enable signal is enabled and to disable the first transistor of the first transistor pair when the first enable signal is not enabled;

The recitation of the second transistor pair has been similarly amended.

Weber does not disclose a second transistor of the first transistor pair that is coupled to receive a first enable signal and is configured to enable the first transistor of

the first transistor pair when the first enable signal is enabled and to disable the first transistor of the first transistor pair when the first enable signal is not enabled. Weber's transistor 14 is described as follows:

> "transistor 14 protects transistor 12 from the high voltage swings that result on the RFout node. Since transistor 14 is connected such that it has a unity current gain, it does not significantly degrade the transconductance of transistor 12 and can tolerate voltage amplitudes at RFout to be 2*Vdd without exceeding its breakdown voltage. Further, the voltage appearing at the source-drain connection between transistors 12 and 14 is a divided version of the RFout voltage, and as such excessive voltage swings do not appear at the junction of transistor 12." (Weber, col. 3, line 60 – col. 4, line 2)

It is clear that transistor 14 is not configured to enable the first transistor of the first transistor pair when the first enable signal is enabled and to disable the first transistor of the first transistor pair when the first enable signal is not enabled, as set forth in amended claim 1. This deficiency is not corrected by the combination of Yamaguchi and Vathulya, because transistor 14 provides a different purpose, as stated above.

For these reasons, claim 1, and claims 2-7 that depend therefrom, are believed to be patentably distinct from the prior art.

3. Claims 8 and 12 were rejected under 35 USC § 103 (a) as being unpatentable over the combination of Weber, Yamaguchi, Vathulya and Hans. In setting forth the rejection, the Examiner again cited Weber as disclosing the first transistor pair of claims 8 and 12 based on transistors (12) and (14) of Weber's Fig. 1. The first transistor pair of Claims 8 and 12 has also been amended in a similar fashion to Claim 1.

As discussed above, Weber's transistor 14 is not configured to enable the first transistor of the first transistor pair when the first enable signal is enabled and to disable the first transistor of the first transistor pair when the first enable signal is not enabled, as set forth in amended claims 8 and 12. This deficiency is not corrected by the combination of Yamaguchi, Vathulya and Hans, because transistor 14 provides a different purpose, as stated above.

For these reasons, claims 8 and 12, and claims 9-11 and 13-15 that depend therefrom, are believed to be patentably distinct from the prior art.

4. Claim 16 was rejected under 35 USC § 103 (a) as being unpatentable over the combination of Weber, Yamaguchi and Vathulya. In setting forth the rejection, the Examiner apparently cited Weber as disclosing the first differential enable transistor pair of claim 16 based on transistor (14) and first differential input transistor pair of claim 16 based on transistor (12) of Weber's Fig. 1. Claim 1, as amended now recites:

> first differential input transistor pair operably coupled to the first differential enable transistor pair, wherein the first differential input transistor pair is, when enabled by the first differential enable transistor pair, operably coupled to amplify a differential input signal at a first gain;

As discussed above, Weber's transistor (12) is not enable by transistor (14). Transistor 14 is provided by Weber for a separate purpose.

For this reasons, claim 16, and claims 17-18 that depend therefrom, are believed to be patentably distinct from the prior art.

For the foregoing reasons, the applicant believes that claims 1-18 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

This response is timely made. The Commissioner is authorized to charge any additional fees that are required or credit any overpayment to Deposit Account No. 50-2126 (Docket BP 2133).

RESPECTFULLY SUBMITTED,

By: /Bruce E. Stuckman/Reg. #36693
Bruce E. Stuckman
Garlick Harrison & Markison, LLP
Phone: (512) 241-8444
Fax No.: (512) 241-8445

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on the date below:

April 3, 2006
Date

Sherry Wolf McWhinnie